3. From Wafer to Panel Level Packaging

Course Leaders: Tanja Braun and Piotr Mackowiak – Fraunhofer IZM

Course Description:
Wafer and Panel Level Packaging are two of the dominating trends in microelectronics packaging. Both approaches with different flavors as RDL last face-up or face-down have reached maturity and are introduced in high volume manufacturing. Main driver for moving from wafer to panel level packaging is of course lowering the packaging cost. More packages can be processed in parallel and panel formats have a much better area utilization (ratio between panel/wafer size and package size) than round wafer shapes. With the advent of chiplet technology and the application to large body size packages e.g. HPC modules Panel Level Packaging is actually gaining momentum as an option for lower cost and high-density packaging. The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging. This will include material and process discussion, technologies, equipment, applications and market trends as well as cost and environmental aspects.

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Course Outline:

1. Introduction Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-out Wafer Level: Material, Processes, Applications
4. Introduction and Definition Panel Level Packaging (PLP)
5. Fan-out Panel Level Packaging: Technologies, Challenges & Opportunities

Who Should Attend:
Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging. Engineers and manages are welcome as detailed technology descriptions as well as market trends, applications and cost modelling are presented.

Bio 1: Tanja Braun studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. In 2013 she received her Dr. degree from the Technical University of Berlin. Tanja Braun is head of the department System Integration and Interconnection Technologies. Recent research is focused on Fan-out Wafer and Panel Level Packaging technologies. In 2021 she received the Exceptional Technical Achievement Award from IEEE Electronics Packaging Society (EPS) and the IMAPS Sidney J. Stein Award for her work in the field of Fan out Wafer and Panel Level Packaging. Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Board of Governor (BOG) and is the IEEE EPS VP of Conferences.

Bio 2: Piotr Mackowiak received his diploma at Technische Universität Berlin 2013. After his thesis he started working at the Microsensor and Actuators Group at the TU-Berlin on MEMS Devices for harsh environment. Since 2016 he is working at Fraunhofer IZM in the Wafer Level System Integration department in the group 3D Integration. His focus of work is the Plasma

etching of silicon and plasma deposition of dielectric layers for TSV Application. In 2018 he joined the microsensors group and focused on SiC sensors and the SiC Via formation. In 2022 he finished his doctoral thesis on Through Silicon carbide Vias. Since 2022 he is heading the group of Microsensor at the Fraunhofer IZM. He has been a visiting scholar at School of microelectronics, Fudan University, Shanghai (2015) and Queensland Micro Nanotechnology Centre, Griffith University, Brisbane (2016). He has authored over 60 conference papers and journal articles.